![Texas Instruments]

TPS62825, TPS62826, TPS62827

ZHCSHY6C −MARCH 2018−REVISED MARCH 2019

# 采用 1.5mm × 1.5mm QFN 封装且具有 1% 输出精度的 TPS6282x、2.4V 至 5.5V 输入、2/3/4A 降压转换器
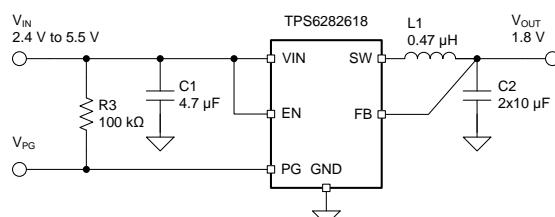
1 特性

- DCS-Control 拓扑
- 1% 反馈或输出电压精度（整个温度范围）
- 效率高达 97%
- 26mΩ 和 25mΩ 内部功率 MOSFET
- 2.4V 至 5.5V 输入电压范围
- 4μA 工作静态电流
- 2.2MHz 开关频率
- 可调输出电压范围为 0.6V 至 4V
- 可实现轻负载效率的省电模式
- 可实现最低压降的 100% 占空比
- 有源输出放电
- 电源正常输出
- 热关断保护
- 断续短路保护
- 使用 TPS6282x 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 固态硬盘
- 便携式电子产品
- 视频监控
- 工业 PC
- 多功能打印机
- 通用负载点

典型应用电路原理图

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3 说明

TPS6282x 是一个易于使用的同步降压直流/直流转换器系列，具有仅 4μA 的极低静态电流。该产品基于 DCS-Control 拓扑，可提供快速瞬态响应。由于具有内部基准，该产品可在 -40°C 至 125°C 的结温范围内以 1% 的反馈电压精度将输出电压调节到低至 0.6V。该系列器件实现了引脚到引脚和 BOM 到 BOM 兼容。整个解决方案需要一个小型 470nH 电感器、一个单 4.7μF 输入电容器以及两个 10μF 或单 22μF 输出电容器。
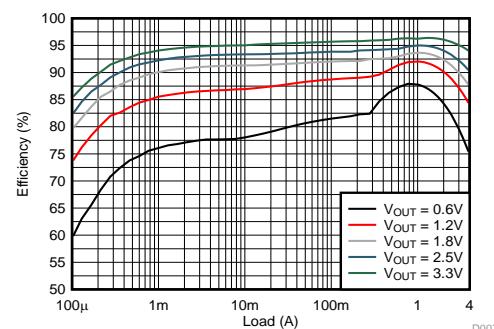
TPS6282x 可自动进入省电模式，在超轻负载条件下保持高效率，从而延长系统电池的运行时间。该器件 具有 电源正常信号和内部软启动电路。它们能够以 100% 模式运行。在故障保护方面，该系列器件加入了断续短路保护以及热关断功能。该器件可采用 6 引脚 1.5 x 1.5mm QFN 封装，提供具有最高功率密度的解决方案。

器件信息[1]

器件号	封装	封装尺寸（标称值）
TPS62825x	6 引脚 VSON-HR	1.5mm x 1.5mm
TPS62826x		
TPS62827x		

[1] 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

V_{IN} = 5V 时的效率

English Data Sheet: SLVSEF9

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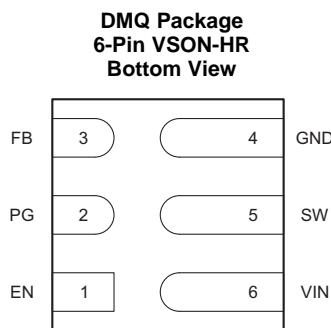
Changes from Revision A (May 2018) to Revision B **Page**

Changes from Original (March 2018) to Revision A **Page**

5   Device Options

PART NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT
TPS62825DMQ	Adjustable	2 A
TPS6282518DMQ	1.8 V	
TPS62826DMQ	Adjustable	3 A
TPS6282618DMQ	1.8 V	
TPS62827DMQ	Adjustable	4 A

6   Pin Configuration and Functions

DMQ Package
6-Pin VSON-HR
Bottom View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	2	O	Power good open drain output pin. The pull-up resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
FB	3	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	4		Ground pin.
SW	5	PWR	Switch pin of the power stage.
VIN	6	PWR	Input voltage pin.

7   Specifications

7.1   Absolute Maximum Ratings[(1)]

		MIN	MAX	UNIT
Voltage at Pins[(2)]	VIN, FB, EN, PG	−0.3	6	V
	SW (DC)	−0.3	V_{IN} + 0.3	
	SW (DC, in current limit)	−1.0	V_{IN} + 0.3	
	SW (AC, less than 10ns)[(3)]	−2.5	10	
Temperature	Operating Junction, T_J	−40	150	°C
	Storage, T_{stg}	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range, TPS62825x and TPS62826x	2.4		5.5	V
	Input voltage range, TPS62827x	2.5		5.5	
V_{OUT}	Output voltage range	0.6		4.0	V
I_{OUT}	Output current range, TPS62825x	0		2	
	Output current range, TPS62826x	0		3	A
	Output current range, TPS62827x[1]	0		4	
I_{SINK_PG}	Sink current at PG pin			1	mA
V_{PG}	Pull-up resistor voltage			5.5	V
T_J	Operating junction temperature	–40		125	°C

(1)   Lifetime is reduced when operating continuously at I_{OUT} = 4 A and the junction temperature > 100 °C.

7.4 Thermal Information

	THERMAL METRIC[1]	TPS6282x, DMQ (6) - JEDEC	TPS62826EVM-794	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.5	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.9	n/a[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	n/a[2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.1	38.6	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2)   Not applicable to an EVM.

7.5 TPS62827 ELECTRICAL CHARACTERISTICS

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.
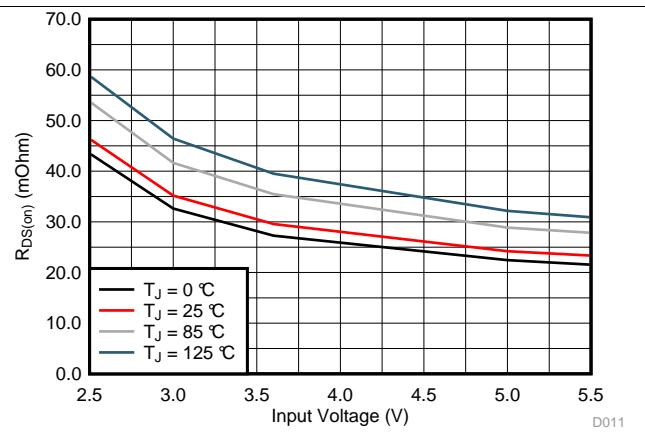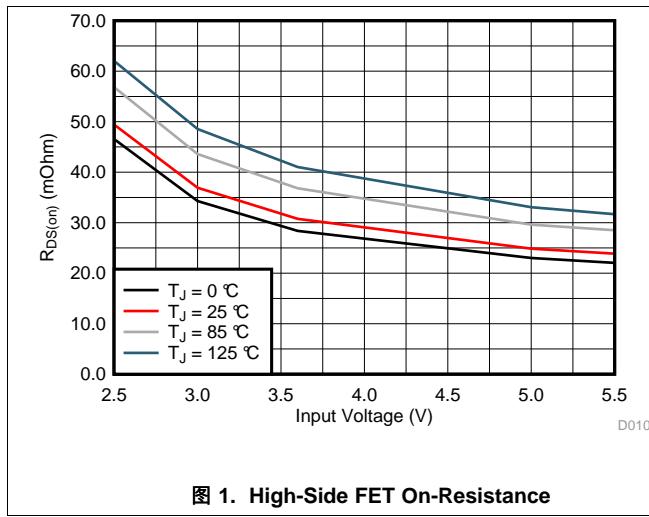
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		4	10	µA
I_{SD}	Shutdown current	EN = Low, T_J = -40 °C to 85 °C		0.05	0.5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level threshold voltage				1.0	V
V_{IL}	Low-level threshold voltage		0.4			V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal, TPS62827		1.75		ms
		Time from EN high to 95% of V_{OUT} nominal, TPS62825/6		1.25		ms

## TPS62827 ELECTRICAL CHARACTERISTICS (continued)
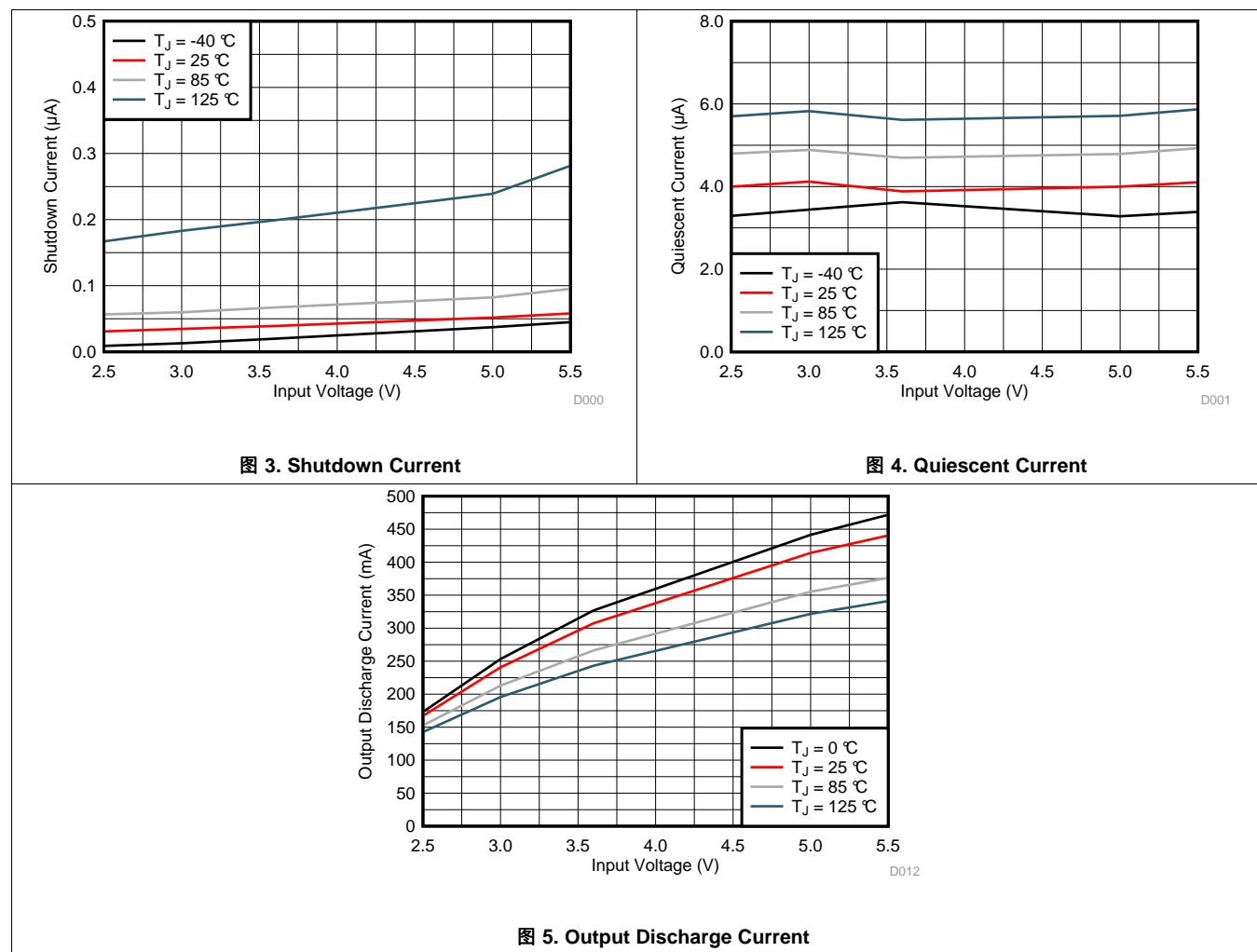
T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94	96	98	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	90	92	94	%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	103	105	107	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	108	110	112	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.1	µA
$t_{PG,DLY}$	Power good deglitch delay	PG rising edge		100		µs
		PG falling edge		20		
OUTPUT						
V_{OUT}	Output voltage accuracy	TPS6282x18, PWM mode	1.78	1.8	1.82	V
V_{FB}	Feedback regulation voltage	PWM mode	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	TPS62825, TPS62826, TPS62827, V_{FB} = 0.6 V		0.01	0.05	µA
R_{FB}	Internal resistor divider connected to FB pin, for fixed output votlage	TPS6282518, TPS6282618		7.5		MΩ
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW	75	400		mA
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{OUT} = 1.8 V		0.1		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ
I_{LIM}	High-side FET switch current limit, DC	TPS62825	2.7	3.3	3.9	A
		TPS62826	3.7	4.3	5.0	A
		TPS62827	4.8	5.6	6.4	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.2		MHz

7.6 Typical Characteristics

图 1. High-Side FET On-Resistance

图 2. Low-Side FET On-Resistance

Typical Characteristics (接下页)

图 3. Shutdown Current

图 4. Quiescent Current

图 5. Output Discharge Current
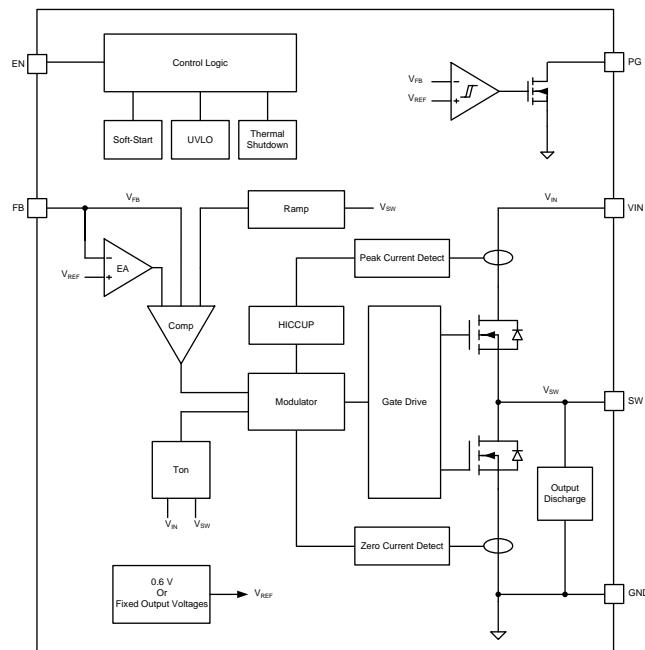
8 Detailed Description

8.1 Overview

The TPS6282x are synchronous step-down converters based on the DCS-Control topology with an adaptive constant on-time control and a stabilized switching frequency. It operates in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Since combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 450ns$$

(1)

8.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the inductor's ripple current. The device operates now with a fixed on-time and the switching frequency further decreases proportional to the load current. It can be calculated as:

Feature Description (接下页)

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \dfrac{V_{IN}}{V_{OUT}} \left[\dfrac{V_{IN} - V_{OUT}}{L} \right]}$$

(2)

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM. The device maintains output regulation in PWM mode.

8.3.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, since even at very low duty cycles the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between VIN and VOUT is determined by the voltage drop across the high-side FET and the dc resistance of the inductor. The minimum VIN that is needed to maintain a specific VOUT value is estimated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L)$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)   (3)

8.3.4 Soft Start

About 250μs after EN goes High, the internal soft-start circuitry controls the output voltage during startup. This avoids excessive inrush current and ensures a controlled output voltage ramp. It also prevents unwanted voltage drops from high-impedance power sources or batteries. TPS6282x can start into a pre-biased output.

8.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from drawing excessive current in case of externally caused over current or short circuit condition. Due to an internal propagation delay (typically 60 ns), the actual ac peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles (about 13μs), the device turns off the high-side MOSFET for about 100μs which allows the inductor current to decrease through the low-side MOSFET's body diode and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

8.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to about 2.2V with a hysteresis of typically 160mV.

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Once the TJ has decreased enough, the device resumes normal operation.

8.4 Device Functional Modes

8.4.1 Enable, Disable and Output Discharge

The device starts operation, when Enable (EN) is set High. The input threshold levels are typically 0.9V for rising and 0.7V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 50nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

8.4.2 Power Good

The TPS6282x has a built in power good (PG) function. The PG pin goes high impedance, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100-μs blanking time and the PG falling edge has a deglitch delay of 20 μs.

表 1. PG Pin Logic

| DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq 0.576$ V	√	
	EN = High, $V_{FB} \leq 0.552$ V		√
	EN = High, $V_{FB} \leq 0.63$ V	√	
	EN = High, $V_{FB} \geq 0.66$ V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	0.7 V $< V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.7$ V	√	

9 Application and Implementation
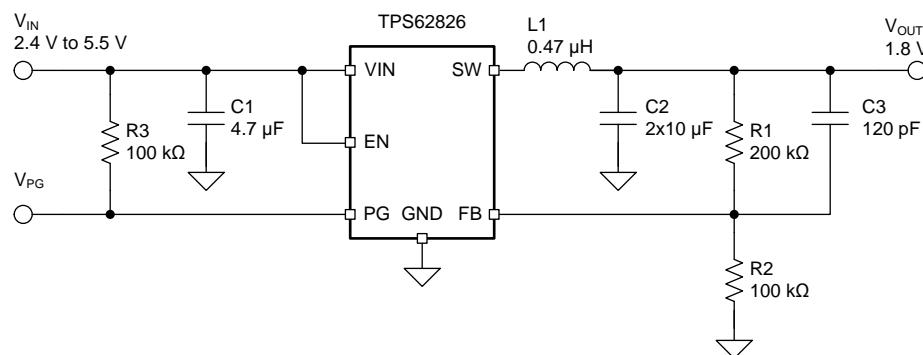
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
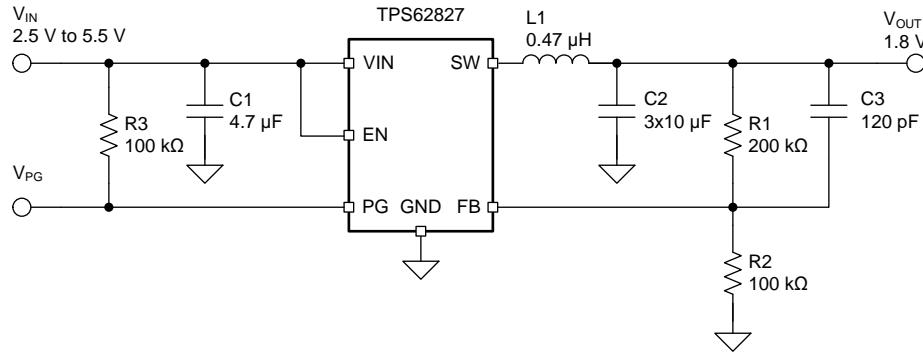
The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

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图 6. **Typical Application of TPS62826**

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图 7. **Typical Application of TPS62827**

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. **Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, TPS62826	2.4 V to 5.5 V
Input voltage, TPS62827	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	<20 mV

Typical Application (接下页)

表 2. Design Parameters (接下页)

DESIGN PARAMETER	EXAMPLE VALUE
Maximum output current, TPS62826	3 A
Maximum output current, TPS62827	4 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2, TPS62826	2 x 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C2, TPS62827	3 x 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C3	120 pF, Ceramic capacitor, 50 V, size 0402	Std
L1	0.47 µH, Power Inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6282x device with the WEBENCH® Power Designer.
1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
• Run electrical simulations to see important waveforms and circuit performance
• Run thermal simulations to understand board thermal performance
• Export customized schematic and layout into popular CAD formats
• Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 公式 4:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

(4)

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. 公式 5 shows how to compute the value of the feed forward capacitor for a given R2 value. For the recommended 100k value for R2, a 120 pF feedforward capacitor is used.

$$C3 = \frac{12\mu}{R2}$$

(5)

For the fixed output voltage versions, connect the FB pin to the output. R1, R2 and C3 are not needed. The fixed output voltage devices have an internal feed forward capacitor.

9.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 4. Matrix of Output Capacitor and Inductor Combinations, TPS62825/6

NOMINAL L [µH][1]	NOMINAL C$_{OUT}$ [µF][2]			
	10	2 x 10 or 22	47	100
0.33				
0.47	+	+[3]	+	
1.0				

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and −30%.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and −35%.
(3) This LC combination is the standard value and recommended for most applications.

表 5. Matrix of Output Capacitor and Inductor Combinations, TPS62827

NOMINAL L [µH][1]	NOMINAL C$_{OUT}$ [µF][2]			
	22	3 x 10	47	100
0.33				
0.47		+[3]	+	+
1.0				

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and −30%.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and −35%.
(3) This LC combination is the standard value and recommended for most applications.

9.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 6 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \dfrac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value   (6)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. 表 6 lists recommended inductors.

表 6. List of Recommended Inductors

Inductance [μH]	Current Rating [A]	Dimensions [L x W x H mm]	MAX. DC Resistance [mΩ]	Mfr Part Number[1]
0.47	4.8	2.0 x 1.6 x 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 x 1.2 x 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 x 1.6 x 1.0	32	DFE201610E - R47M, MuRata
	4.8	2.0 x 1.6 x 1.0	32	DFE201210S - R47M, MuRata
	5.1	2.0 x 1.6 x 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 x 1.6 x 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 x 4.0 x 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 x 3.2 x 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 x 4 x 1.8	11.2	WE-LHMI-744373240047, Würth

(1) See *Third-party Products Disclaimer*

9.2.2.5 Capacitor Selection
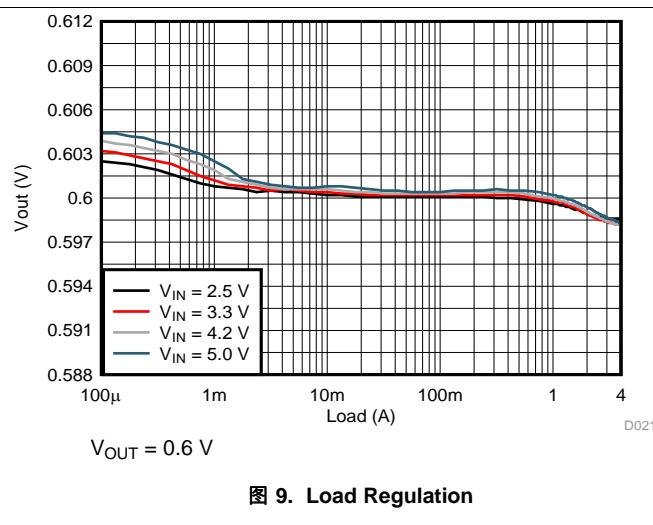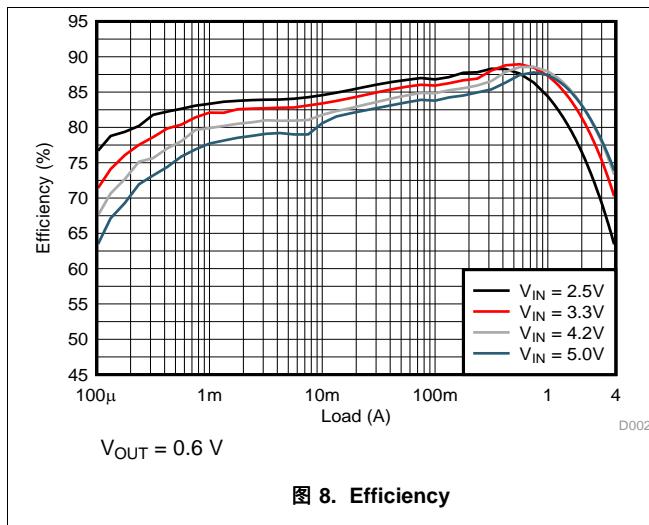
The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, a minimum effective input capacitance of 3 μF should be present, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. Considering the DC-bias derating the capacitance, the minimum effective output capacitance is 10 μF for TPS62825/6 and 20 μF for TPS62827.

A feed forward capacitor is required for the adjustable version, as described in *Setting The Output Voltage*. This capacitor is not required for the fixed output voltage versions.

9.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

V_{OUT} = 0.6 V

图 8. Efficiency

V_{OUT} = 0.6 V

图 9. Load Regulation

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

V_{OUT} = 1.2 V

图 10. Efficiency

V_{OUT} = 1.2 V
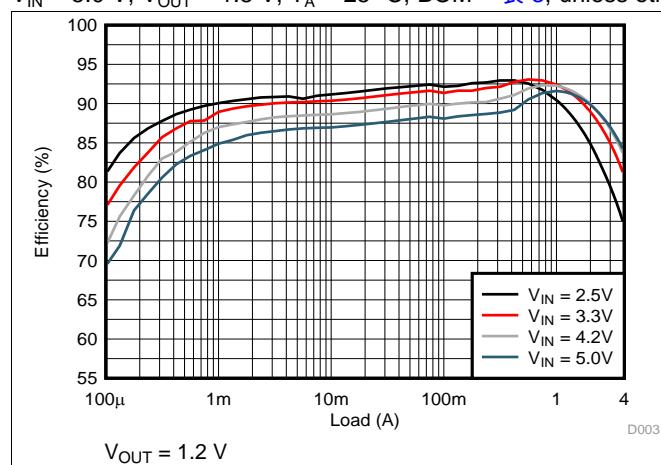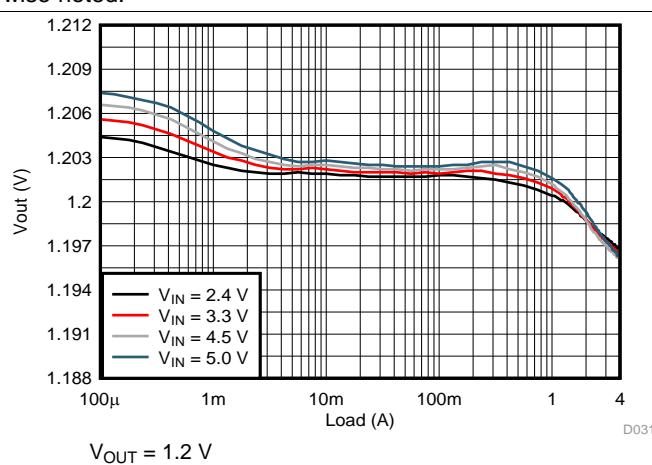
图 11. Load Regulation
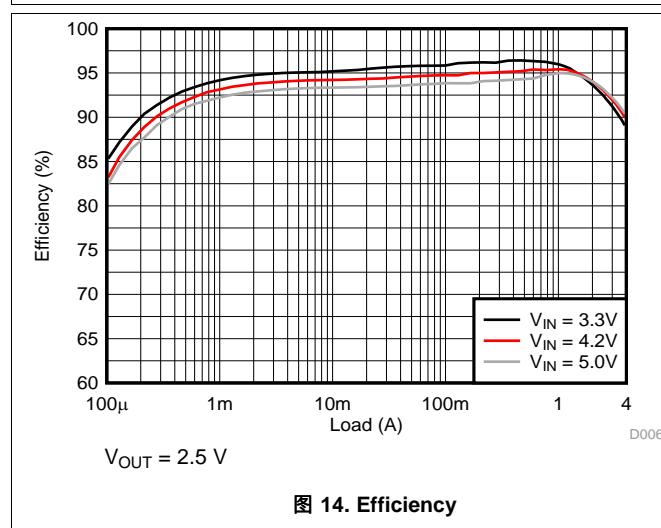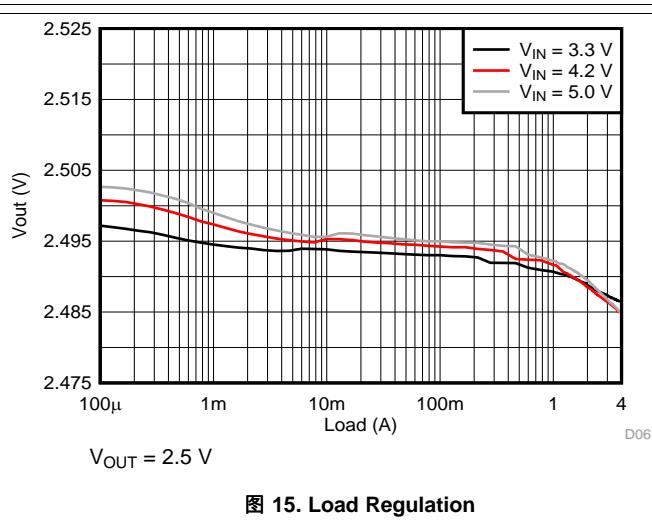
V_{OUT} = 1.8 V

图 12. Efficiency

V_{OUT} = 1.8 V

图 13. Load Regulation

V_{OUT} = 2.5 V

图 14. Efficiency

V_{OUT} = 2.5 V

图 15. Load Regulation

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

V_{OUT} = 3.3 V

图 16. Efficiency

V_{OUT} = 3.3 V

图 17. Load Regulation

V_{IN} = 3.3 V   TPS62825/6
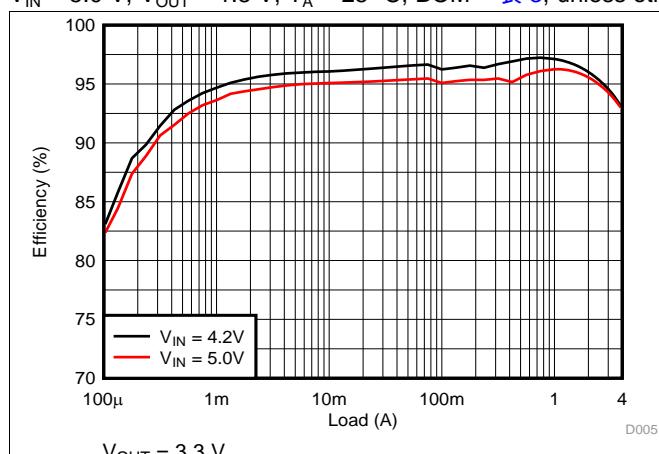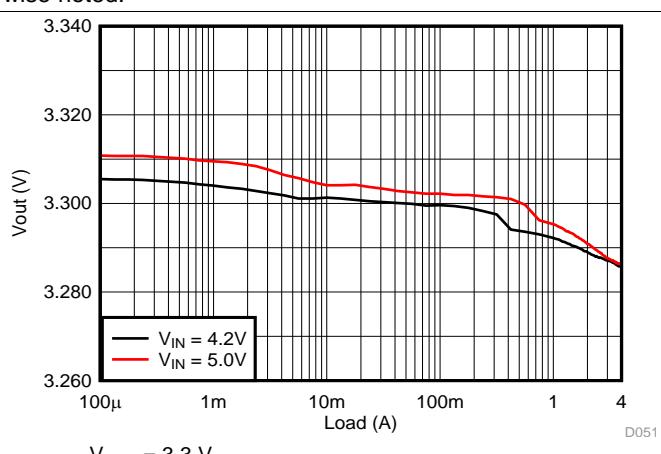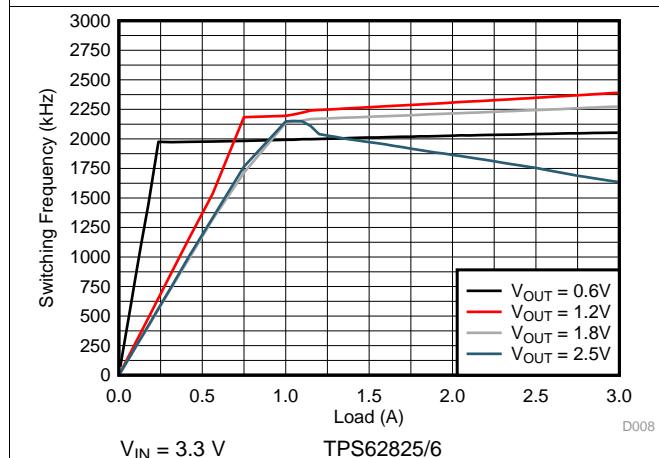
图 18. Switching Frequency

I_{OUT} = 1.0 A   TPS62825/6
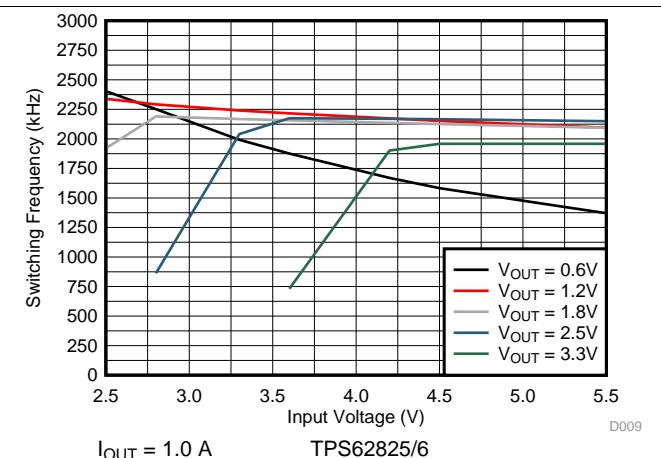
图 19. Switching Frequency

V_{IN} = 3.3 V   TPS62827
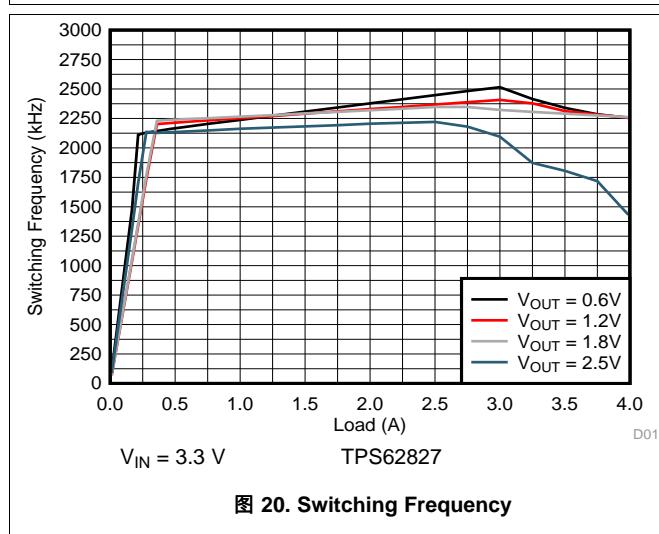
图 20. Switching Frequency

I_{OUT} = 1.0 A   TPS62827
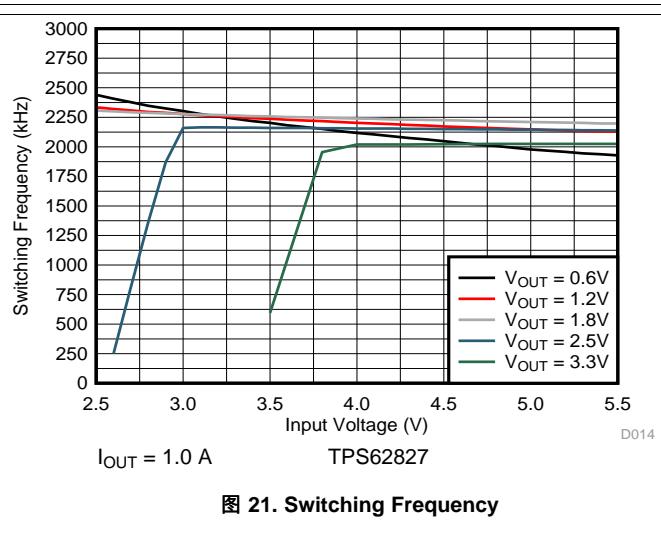
图 21. Switching Frequency

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

V_{OUT} = 1.2 V θ_{JA}= 71.4 °C/W
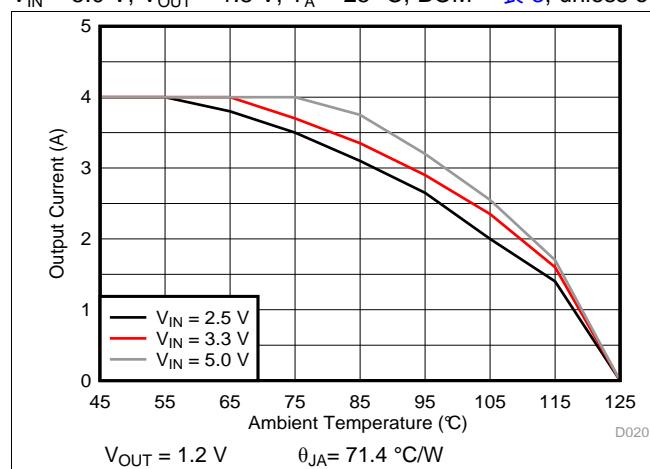
图 22. Thermal Derating

V_{OUT} = 1.8 V θ_{JA}= 71.4 °C/W
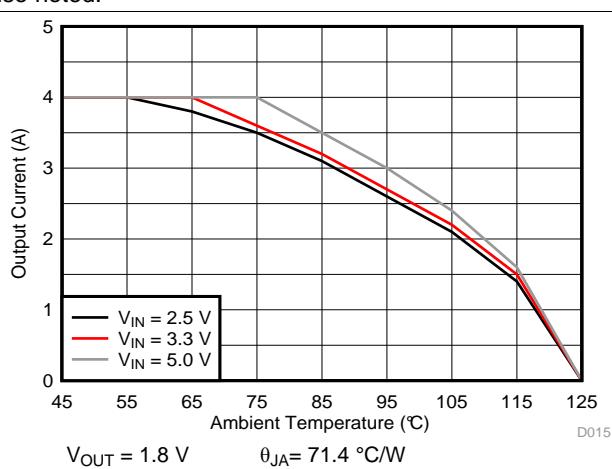
图 23. Thermal Derating

V_{OUT} = 2.5 V θ_{JA}= 71.4 °C/W
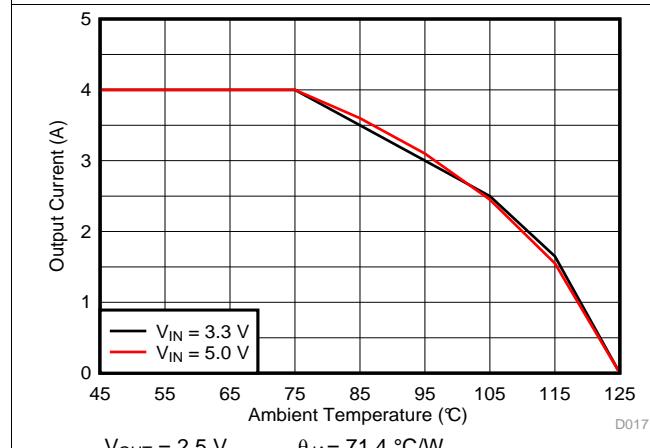
图 24. Thermal Derating

V_{OUT} = 3.3 V θ_{JA}= 71.4 °C/W

图 25. Thermal Derating

I_{OUT} = 1.0 A   TPS62825/6

图 26. PWM Operation

I_{OUT} = 0.1 A   TPS62825/6
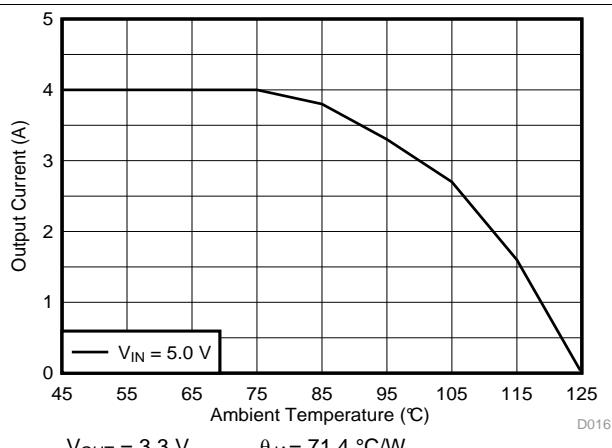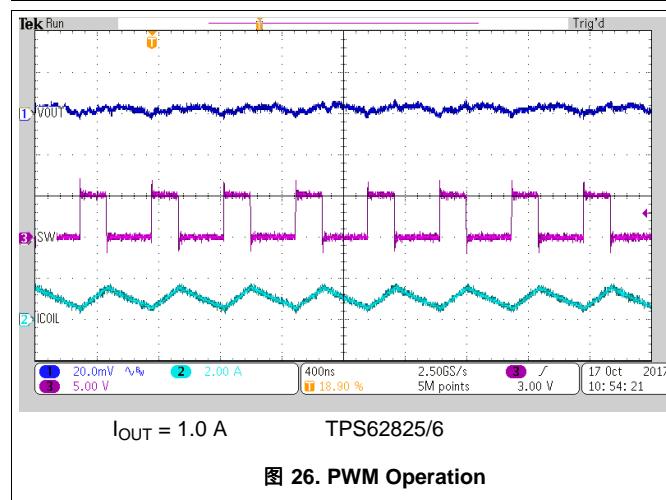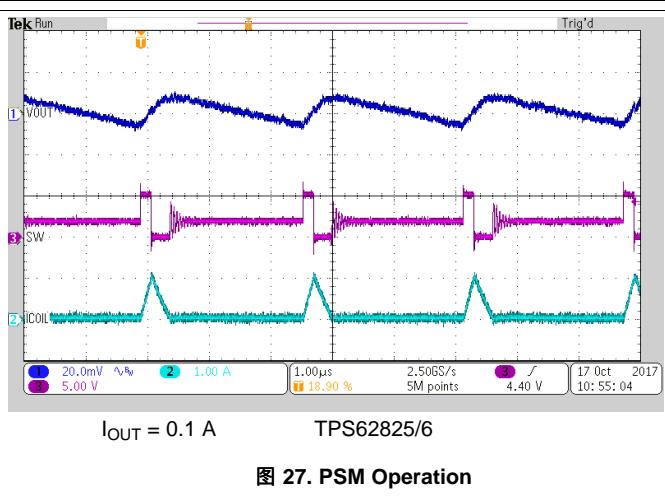
图 27. PSM Operation

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

Load = 0.6 Ω   TPS62825/6
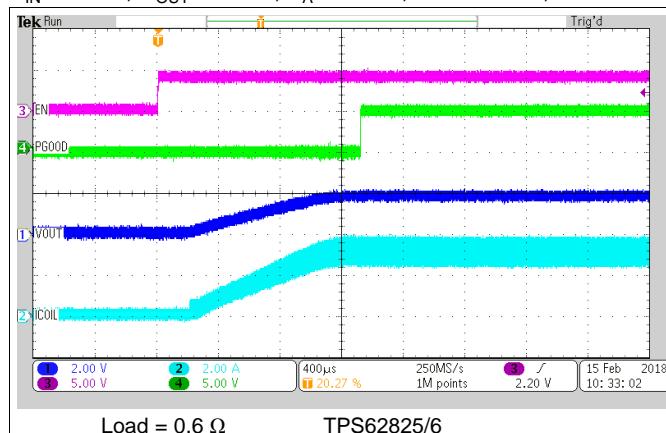
图 28. Startup with Load

TPS62825/6
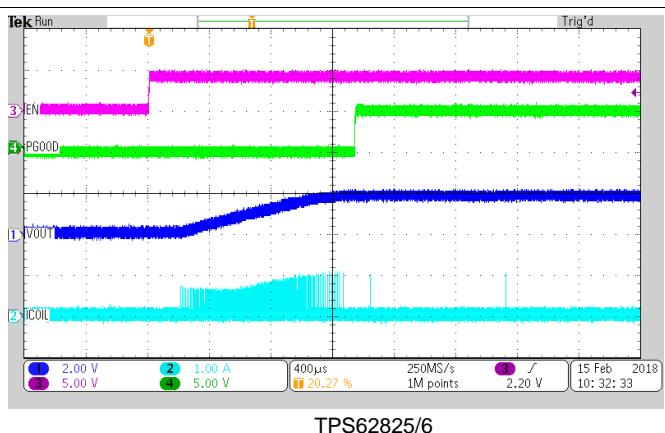
图 29. Startup with No Load

Load = 1.8 Ω   TPS62825/6
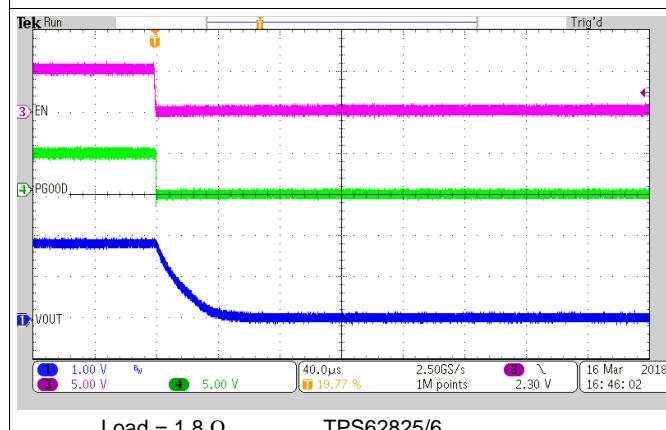
图 30. Disable, Active Output Discharge

TPS62825/6
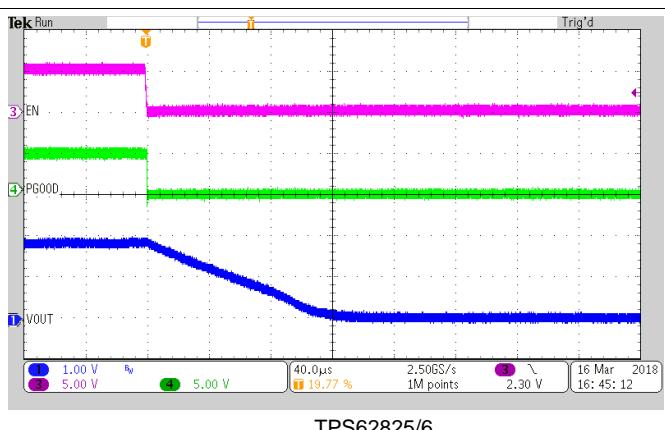
图 31. Disable, Active Output Discharge at No Load

I_{OUT} = 0.05 A to 1A   TPS62825/6
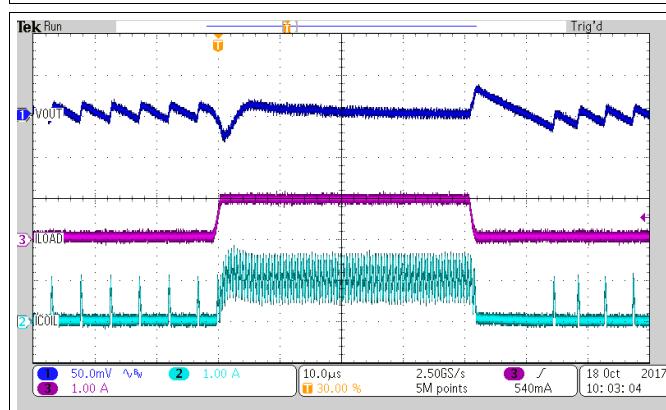
图 32. Load Transient

I_{OUT} = 1 A to 2 A   TPS62825/6
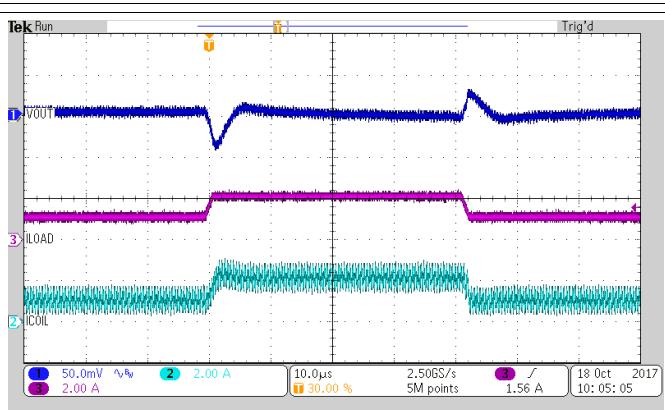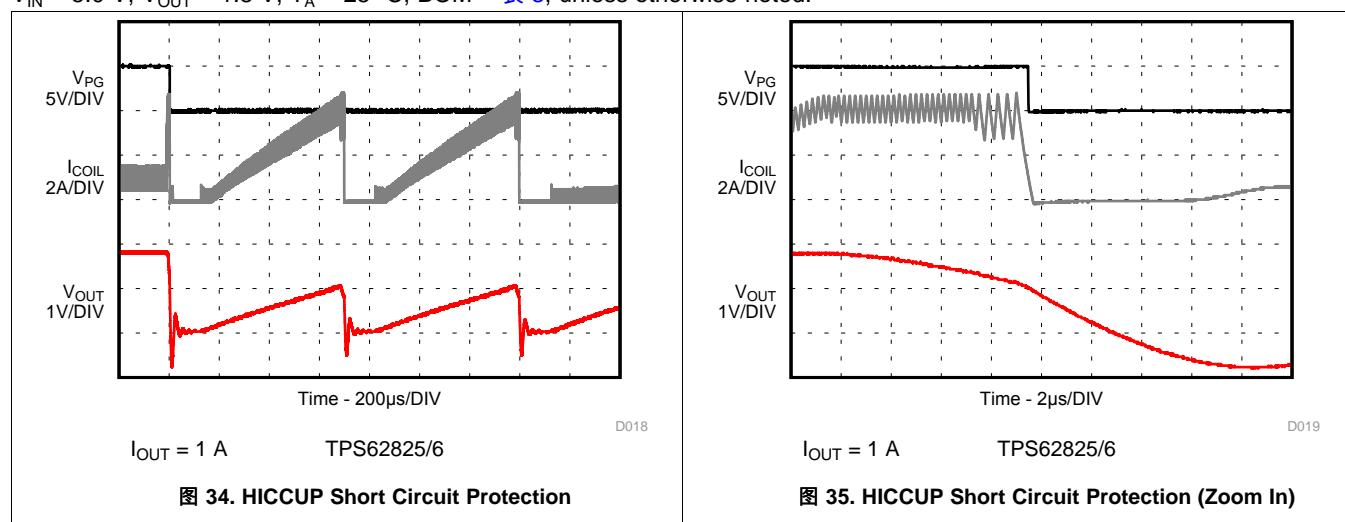
**图 33. Load Transient**

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25 ºC, BOM = 表 3, unless otherwise noted.

I_{OUT} = 1 A   TPS62825/6

图 34. HICCUP Short Circuit Protection

I_{OUT} = 1 A   TPS62825/6

图 35. HICCUP Short Circuit Protection (Zoom In)

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See 图 36 for the recommended PCB layout.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors should be made at the output capacitor.
- Refer to 图 36 for an example of component placement, routing and thermal design.

11.2 Layout Example
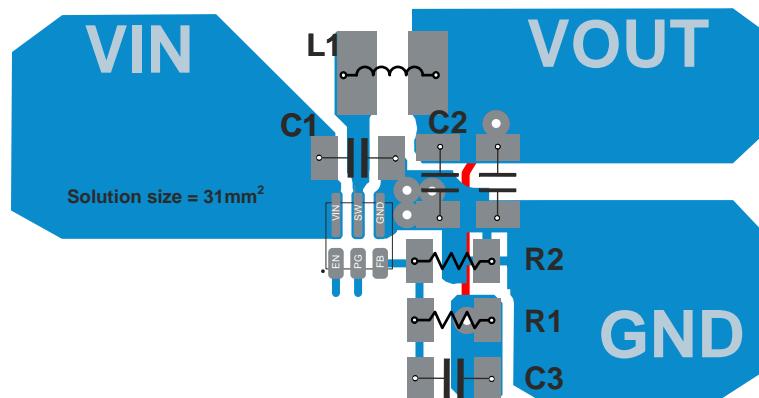
图 36. PCB Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:
- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in *Thermal Information* provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, SZZA017 and SPRA953.

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.1.2 开发支持

12.1.2.1 使用 *WEBENCH*® *工具创建定制设计*

单击此处，使用 TPS6282x 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：
- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：
- 《热工特性应用手册》，SZZA017
- 《热工特性应用手册》，SPRA953

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 7. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TPS62825	单击此处	单击此处	单击此处	单击此处	单击此处
TPS62826	单击此处	单击此处	单击此处	单击此处	单击此处
TPS62827	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TEXAS INSTRUMENTS

www.ti.com

20-Jul-2019

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6282518DMQR	ACTIVE	VSON-HR	DMQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
TPS6282518DMQT	ACTIVE	VSON-HR	DMQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
TPS62825DMQR	ACTIVE	VSON-HR	DMQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
TPS62825DMQT	ACTIVE	VSON-HR	DMQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
TPS6282618DMQR	ACTIVE	VSON-HR	DMQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
TPS6282618DMQT	ACTIVE	VSON-HR	DMQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
TPS62826DMQR	ACTIVE	VSON-HR	DMQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
TPS62826DMQT	ACTIVE	VSON-HR	DMQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
TPS62827DMQR	ACTIVE	VSON-HR	DMQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EH	Samples
TPS62827DMQT	ACTIVE	VSON-HR	DMQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
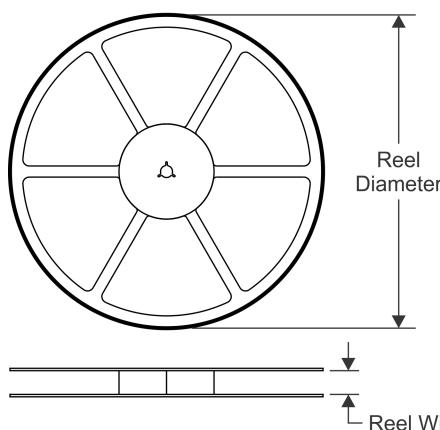
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
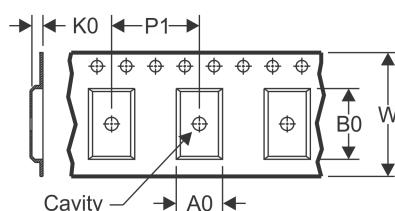
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
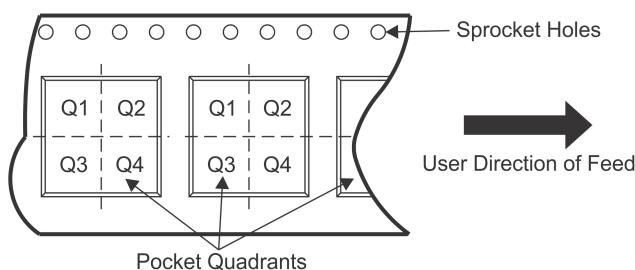
TAPE DIMENSIONS
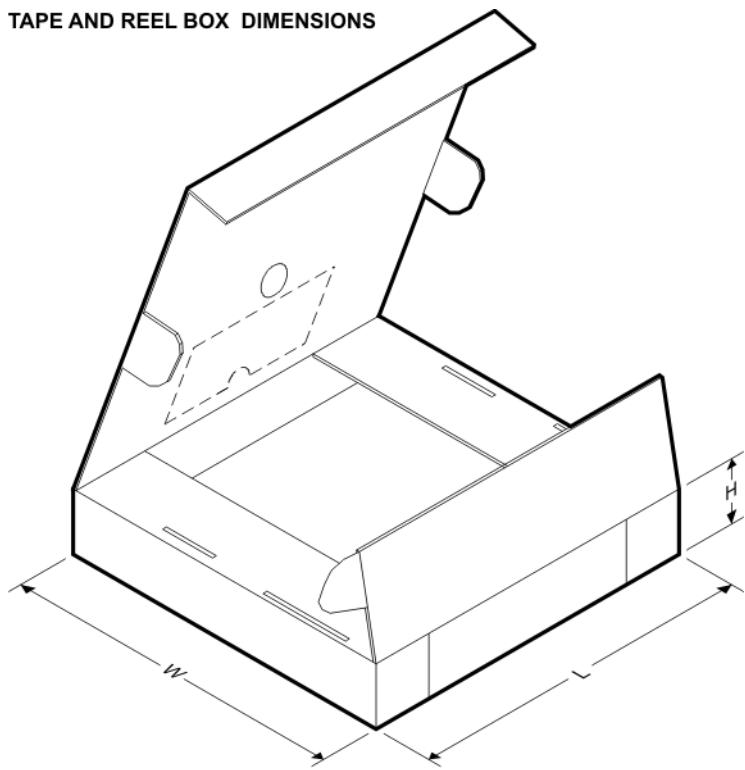
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6282518DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS6282518DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62825DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62825DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS6282618DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS6282618DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62826DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62826DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62827DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS62827DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6282518DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS6282518DMQT	VSON-HR	DMQ	6	250	182.0	182.0	20.0
TPS62825DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS62825DMQT	VSON-HR	DMQ	6	250	182.0	182.0	20.0
TPS6282618DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS6282618DMQT	VSON-HR	DMQ	6	250	182.0	182.0	20.0
TPS62826DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS62826DMQT	VSON-HR	DMQ	6	250	182.0	182.0	20.0
TPS62827DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS62827DMQT	VSON-HR	DMQ	6	250	182.0	182.0	20.0
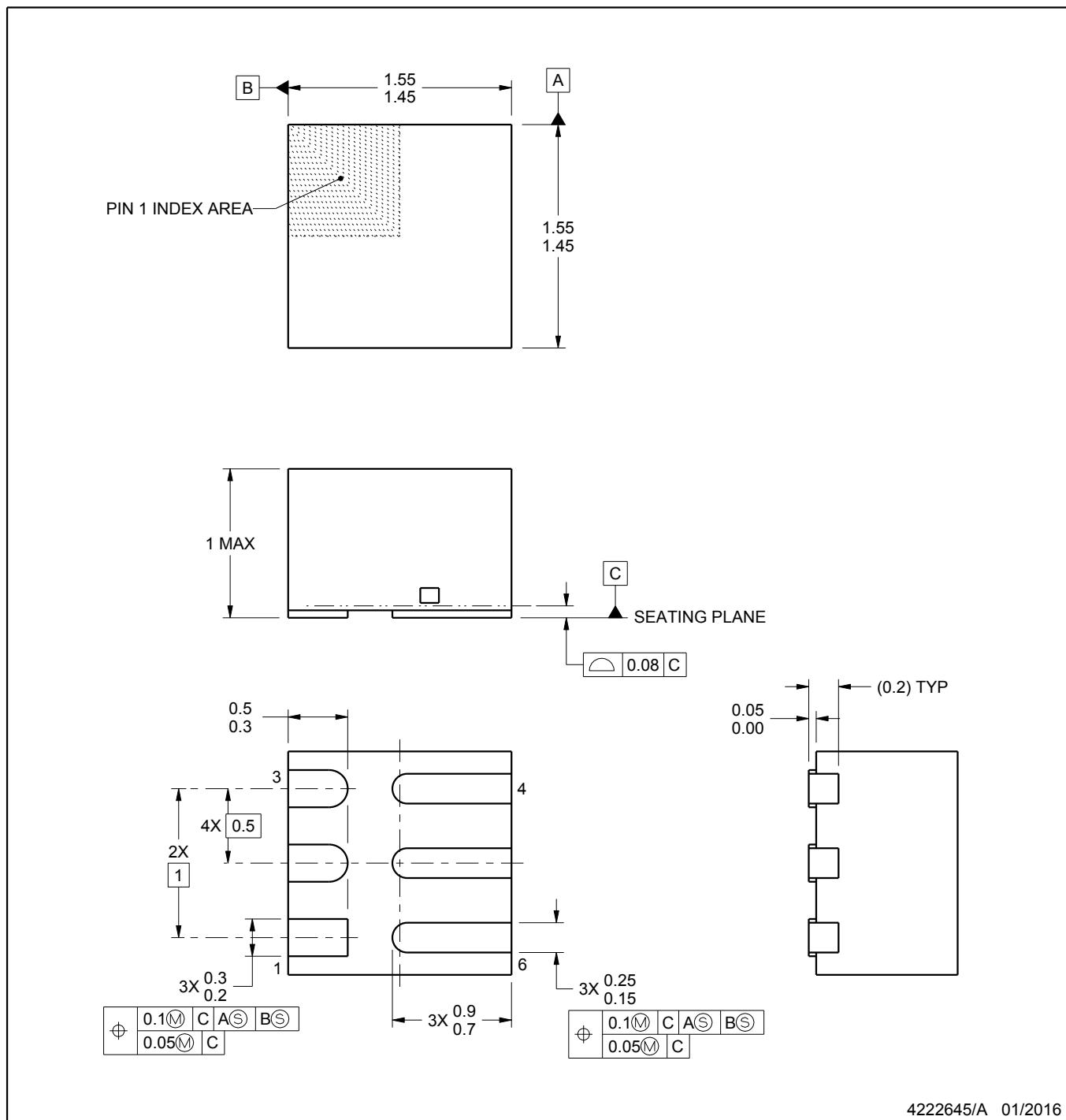
1.55
1.45

B

A

PIN 1 INDEX AREA

1.55
1.45

1 MAX

C

SEATING PLANE

◯ 0.08 C

0.5
0.3

0.05
0.00

(0.2) TYP

3

4

4X 0.5

2X
1

1

6

3X 0.3
0.2

3X 0.25
0.15

3X 0.9
0.7

⊕ | 0.1 Ⓜ | C | A Ⓢ | B Ⓢ
  | 0.05 Ⓜ | C

⊕ | 0.1 Ⓜ | C | A Ⓢ | B Ⓢ
  | 0.05 Ⓜ | C

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NOTES:
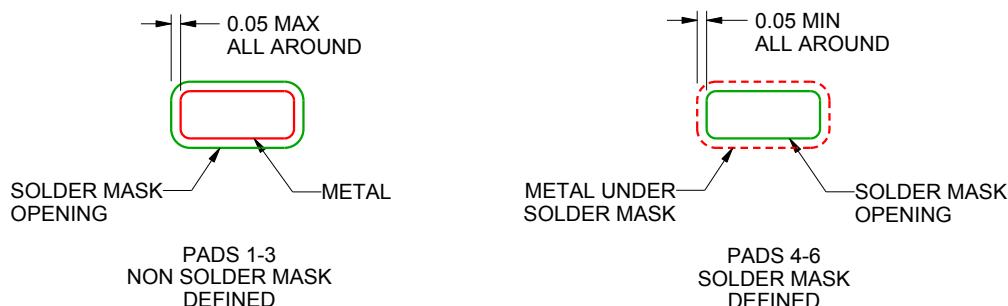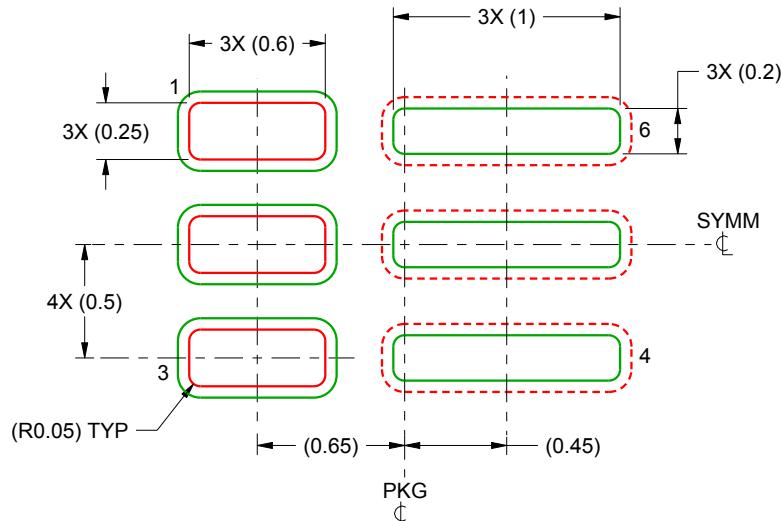
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
SCALE:30X

0.05 MAX
ALL AROUND

SOLDER MASK OPENING

METAL

PADS 1-3
NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

PADS 4-6
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)
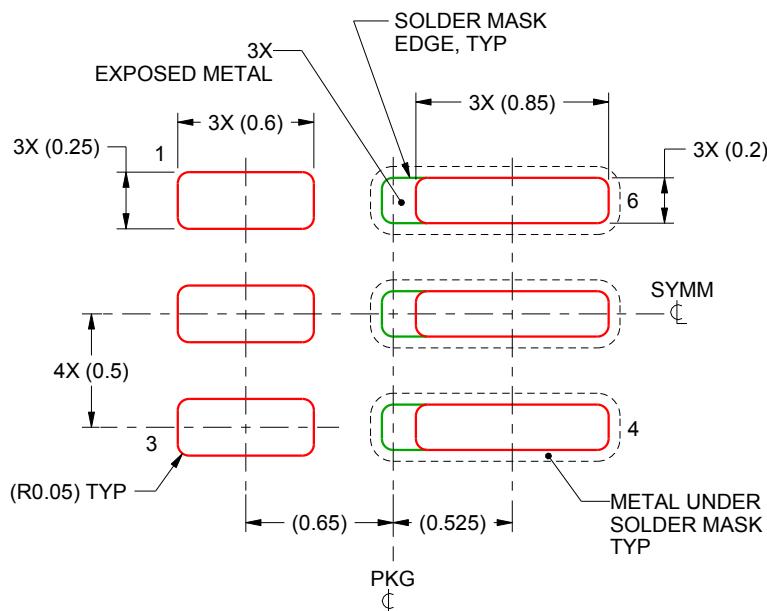
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 4, 5 & 6:
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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